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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/956,903	09/21/2001	Thomas D. Fletcher	2207/11270	2661

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/956,903	FLETCHER, THOMAS D.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/21/01; 02/28/02; 11/18/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/21/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/28/02; 11/18/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 11/18/2002 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. The cited foreign patent document (JP 5-259893 by Furuki) is not provided. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-3, 15-19, and 25-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 1, the limitation "the load" in lines 2-3 lacks an antecedence basis. For examination purposes, the examiner considers "the load" as "a load".

Re claim 2, the limitation "the output" in lines 2-3 lacks an antecedence basis. For examination purposes, the examiner considers "the output" as the true carry generate output and the compliment carry generate output respectively.

Re claim 15, the cited limitations are unclear compare to the drawing in Figure 1. For instant, Figure 1 discloses a first transistor (151) with a source is connected to the

second output (compliment carry generate) and a drain is connected to the source of second transistor (152) instead of a drain is connected to the second output and a source is connected to the drain of the second transistor. For examination purposes, the examiner disregards these limitations cited in the claim.

Re claim 25, the limitations "processing the true input...stacks of transistors" in lines 5-14 are mis-descriptive because the first evaluation block is used to process the true input values and output a complement carry generate value; the second evaluation block is used to process the complement input values and output a true carry generate value as seen in Figure 1. For examination purposes, the examiner considers the limitation in reverse order as the first evaluation block is used to process the true input values and output a complement carry generate value; the second evaluation block is used to process the complement input values and output a true carry generate value.

Thus, claims 3, 16-19, and 26-30 are also rejected for being dependent on the rejected base claims 1, 15, and 25 respectively.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-15 and 20-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Winters (U.S. 6,292,818).

Re claim 1, Winters discloses in Figures 3 and 6 an apparatus comprising a symmetric differential domino (col. 3 lines 22-24) carry generate circuit (Figure 6) having true inputs (e.g. A1H, B1H, ...) and compliment inputs (e.g. A1L, B1L...), wherein the load for the true inputs is equal to the load for the compliment inputs (Figure 6).

Re claim 2, Winters further discloses in Figures 3 and 6 the circuit also has a true carry generate output (24 as CAR) and a compliment carry generate output (the other output), and wherein the output drive strength for true output is the same as the output drive strength for compliment output (Figure 6).

Re claim 3, Winters further discloses in Figures 3 and 6 the circuit further comprises: a first evaluation block (transistors that have A1H, B1H, and C1H as inputs) having a plurality of transistors, wherein a number p of transistors are connected in a parallel relationship (e.g. transistor of A1H and C1H) and a number of transistors are connected in a serial relationship (e.g. transistor of A1H and B1H); and a second evaluation block (transistors that have A1L, B1L, and C1L as inputs) having a plurality of transistors, wherein in the second evaluation block p transistors connected in a parallel relationship (e.g. transistor of A1L and C1L as A1L) and transistors connected in a serial relationship (e.g. transistor of A1L and B1L).

Re claim 4, Winters discloses in Figures 3 and 6 an apparatus comprising a differential domino carry generate circuit having a first evaluation block of switches

(transistors that have A1H, B1H, and C1H as inputs) and a second evaluation block of switches (transistors that have A1L, B1L, and C1L as inputs), wherein the first evaluation block and second evaluation block each have the same number switches connected in parallel and each have the same number of transistors connected in series (they are mirror).

Re claim 5, Winters further discloses in Figures 3 and 6 the switches in the first evaluation block and second evaluation block are N-channel metal-oxide semiconductor (NMOS) transistors (Figure 6).

Re claim 6, Winters further discloses in Figures 3 and 6 corresponding transistors in the first evaluation block and second evaluation block are the same size (they are mirror and total transistors in each block is 6).

Re claim 7, Winters further discloses in Figures 3 and 6 the apparatus further comprises cross-coupled P-channel metal-oxide semiconductor (PMOS) keeper transistors (transistors that poll VDD).

Re claim 8, Winters further discloses in Figures 3 and 6 the differential domino carry generate circuit is a first stage in a carry look-ahead adder (abstract and Figure 3).

Re claim 9, Winters further discloses in Figures 3 and 6 the differential domino carry generate circuit is a group generate gate (abstract).

Re claim 10, Winters discloses in Figures 3 and 6 an apparatus comprising: a first output to provide a pre-charge value (26) during a pre-charge phase and a true carry generate value driving an evaluation phase (transistors that have A1H, B1H, and C1H as inputs); a second output to provide the pre-charge value (25) during the pre-charge phase

and the compliment of the true carry generate true during the evaluation phase (transistors that have A1L, B1L, and C1L as inputs); a current input (VDD); a first evaluation block (transistors that have A1H, B1H, and C1H as inputs) connected to the current input and the first output and having a plurality of transistors, wherein a number of transistors are connected in a parallel relationship and a number of transistors are connected in a serial relationship; and a second evaluation block connected to the current input and the second output and having a plurality of transistors, wherein the second evaluation block (transistors that have A1L, B1L, and C1L as inputs) has the same number of transistors connected in a parallel relationship as the first evaluation block and the same number of transistors connected in a serial relationship as the first evaluation block (left portion in Figure 6 is mirror the right portion of Figure 6).

Re claim 11, Winters further discloses in Figures 3 and 6 the output drive strength for the first output is the same as the output drive strength for the second output (same VDD in the pre-charge in Figure 6).

Re claim 12, Winters further discloses in Figures 3 and 6 the current input is a transistor having a source node connected to ground and a gate connected to the clock input (e.g. transistor at C1H in Figure 6).

Re claim 13, Winters further discloses in Figures 3 and 6 circuit further comprises a clock input to receive a clock having pre-charge and evaluation phases (C1L and C1H).

Re claim 14, Winters further discloses in Figures 3 and 6 the gate of each transistor in the first evaluation block (transistors that have A1H, B1H, and C1H as inputs) is connected to one of a set of true inputs and the gate of each of the transistors in

the second evaluation block (transistors that have A1L, B1L, and C1L as inputs) is connected to one of a set of compliment inputs, and wherein the load for the true inputs is the same as the load for the compliment inputs (Figure 6).

Re claim 15, Winters further discloses in Figures 3 and 6 the first evaluation block comprises a first transistor with a drain connected to the second output, a second transistor with a drain connected to the source of the first transistor and a source connected to the current input, a third transistor with a drain connected to the second output, a fourth transistor with a drain connected to the source of the third transistor and a source connected to the current input, and a fifth transistor with a drain connected to the source of the fourth transistor and a source connected to the second output (Figure 6 with transistors that have A1H, B1H, and C1H as inputs).

Re claim 20, it has similar limitations cited in claim 10. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 21, it has similar limitations cited in claim 11. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 22, it has similar limitations cited in claim 15. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 15.

Re claim 23, Winters further discloses in Figures 3 and 6 the gate of the first transistor is connected to an exclusive-OR input, the gate of the second transistor is connected to a first generate input, the gate of the third transistor is connected to a compliment exclusive-OR input, the gate of the fourth transistor is connected to a second

generate input, and the gate of the fifth transistor is connected to a propagate input (e.g. equations 5-6 in col. 4 lines 1-4).

Re claim 24, Winters further discloses in Figures 3 and 6 the transistors in the first evaluation block and second evaluation block are N-channel metal-oxide semiconductor (NMOS) transistors (NMOS in Figure 6).

Re claim 25, it is a method claim of claim 10. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 26, Winters further discloses in Figures 3 and 6 the first evaluation block and second evaluation block have corresponding stacks that have the same number of transistors (for each the total transistors is 6).

Re claim 27, Winters further discloses in Figures 3 and 6 the method receiving a clock (C1L and C1H) having a pre-charge phase (transistors at 25 and 26) and an evaluation phase (Figure 6); providing pre-charge values at the first output and at the second output during pre-charge phase; and providing the carry generate value at the first output and the compliment carry generate value at the second output during the evaluation phase (output of Figure 6).

Re claim 28, Winters further discloses in Figures 3 and 6 the method further comprises preventing current from passing through the current input during the precharge phase and enabling current to pass through the current input during the evaluation phase (e.g. 25 and 26).

Re claim 29, Winters further discloses in Figures 3 and 6 the method further comprises: providing the output from the first evaluation block to a keeper (left VDD

power source in Figure 6); providing the output from the second evaluation block to a keeper (right VDD power source in Figure 6); and providing the carry generate true output (output of 25) and carry generate compliment output (output of 26) during the evaluation phase based upon output from the first evaluation block (High inputs block), second evaluation block (Low input block), and the keeper (two VDD transistors).

Re claim 30, Winters further discloses in Figures 3 and 6 the inputs received and outputs provided are symmetrical (the left portion is mirror the right portion as seen in Figure 6).

Allowable Subject Matter

6. Claims 16-19 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,450,340 to Nicolaidis discloses an implementation technique of self-checking arithmetic operators and data paths based on double-rail and parity codes.

b. U.S. Patent No. 6,466,960 to Winters disclose a method and apparatus for performing a sum and compare operation.

c. U.S. Patent No. 5,880,986 to Dedhia discloses a method and apparatus for reducing power usage within a domino logic unit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

August 24, 2004

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